1972

Design and Construction of a Digital Pulse Generator

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DESIGN AND CONSTRUCTION OF A DIGITAL PULSE GENERATOR

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June 1972
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ABSTRACT

This pulse generator was built to complement the Stroboscope 501, a high speed multi-flash unit capable of producing up to 6000 flashes per second. The Stroboscope is equipped with a electro-mechanical frequency generator, however a solid state pulse generator has the advantages of being highly accurate and repeatable. The basic design criteria were that the generator have several selectable frequencies within the limit of the Stroboscope, be able to count several different amounts of pulses and then close off automatically and be triggerable from an exterior source.The unit designed meets all these specifications. A high speed multi-flash strobe has applications in scientific photography where any high speed operation must be photographed. Examples are a photograph of a bullet leaving the barrel of a rifle or a piece of machinery operating at high speed.

INTRODUCTION

This research project involved the design and construction of a digital pulse generator. It was desired that the Stroboscope '501' have an exterior and independent triggering device. This trigger system was to be in addition to the existing internal trigger of the Stroboscope. An electronic triggering system offers the advantages of great accuracy and repeatability in terms of frequency and pulses produced. The generator is essentially an information handling system, the information being a steady supply of pulses which are processed in order to obtain a triggering of the flash in the desired manner. The core of the research and the project is therefore in the digital processing section of the generator. It is in this area that the most extensive research and design was done. It was necessary to learn the operation of digital intergrated circuits and the methology of digital processing systems. This project served to culminate several Electrical Engineering courses in an electronic system that has useful application in photography.

CIRCUIT DESIGN

The circuit construction and operation can be divided into three distinct sections, the voltage regulator, oscillator and the frequency synthesizer. Each section will be discussed seperately with consideration given as how it fits into the whole operation.

Voltage Regulator

The decision to include a voltage regulator was necessitated by the considerably demanding voltage requirements of the intergrated circuits which operate in the range of from 4.75 to 5.25 volts. This regulator effectively isolates the I.C.s from any major voltage drop in the line input and will also supply a constant voltage with varying load impedances. A simple zener diode type regulator would not prove sufficient in that greater stability is desired. Due to the extensive amount of circuits available for this purpose a predesigned circuit was chosen and utilized, (figure 1)[1]. In addition to its regulatory operation this circuit protects the I.C.s from any high input voltage since the input to the regulator is only 8.5 volts. If a pass transistor should fail and the total input voltage fall across the load it would not prove critical to the I.C.s.

This circuit tends to restore a drop in output voltage from the preset 5 volts by two mechanisms. The first is as follows; a drop in the output causes the base of Q3 to see a more positive potential and thereby causes it to conduct less current. This in turn reduces the base current to Q4, whose reduced collector current allows more base current to reach Q5. Conduction is thereby increased in Q5 and the voltage drop from point A to point B increases. The second mechanism is again started by Q3's reduced conduction allowing more current from R1 to pass through Q2. This in turn causes Q1b and then Q1a to boost their collector currents and drive more current across the zener diode which tends to restore any lost output voltage.

1. T.K. Hemingway, British Aircraft Corp., London
   Electronics Dec. 21 1970, page 54

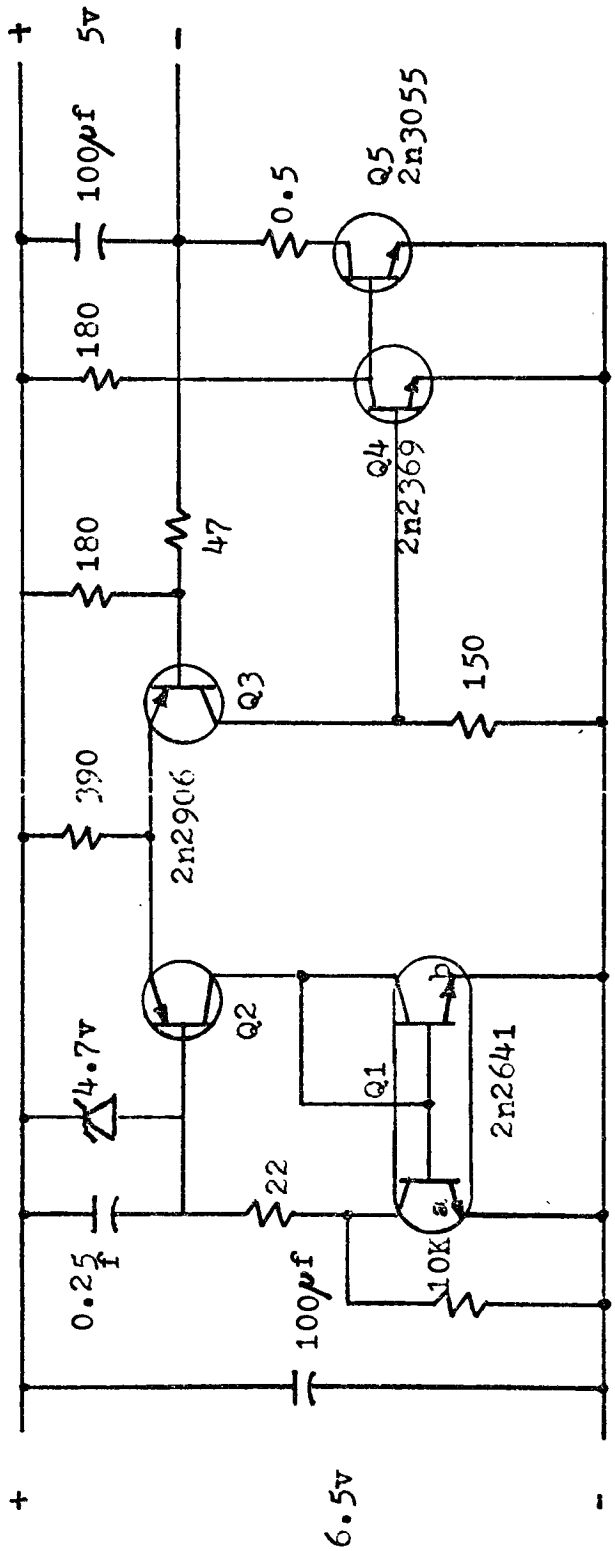


Figure 1 Voltage Regulator

Oscillator

This circuit is a conventional emitter-coupled multivibrator however the usual capacitor has been replaced by a crystal. The output of transistor Q2 is used to vibrate the crystal which will oscillate at its frequency of 100 K hz. This forces the whole circuit to oscillate at that frequency. Square waves are produced since the output is essentially a clipped sine wave due to the fact that the feedback causes the circuit to be overdriven.

I.C. Circuit

Within this circuit the squarewaves pulses produced in the oscillator are programmed according to the desired frequencies and the number of pulses. The I.C. board and its functions are divided into two seperate units, the frequency synthesizer and the pulse counter/ trigger,(figure 3).

The frequency synthesizer generates all the frequencies by dividing the primary oscillator frequency of 1851 Khz. There are two dividing I.C. components, I.C.1, a four bit binary counter and I.C.2 a binary coded decimal decade counter along with I.C.3 a B.C.D. to decimal decoder. The incoming primary frequency passes through I.C. 1 first where depending on the position of switch SW1 it will be divided by factors of 4,8 or 16. Following this division the pulses are sent to I.C.2 which can divide in B.C.D. from 1 to 10 and in decimal by decoding through I.C.3. Switch SW2 can select division factors of 6,7,8,9 or 10, positions 2 through 5 were not used since they would result in repetative freqencies. The total frequency range is shown in table 1 along with the appropriate switch positions.

The pulse counter and trigger compose the other half of the I.C. board. The pulses from the frequency synthesizer must pass through a gate before they reach the output. This gate in turn is controlled by two other I.C.s which constitute the pulse counter. The actual gate is two nor gates tied together (figure 4) that will pass pulses to the output as long as input A is at logical 0. However as soon as it goes to logical 1 the nor gate output will remain at zero volts until

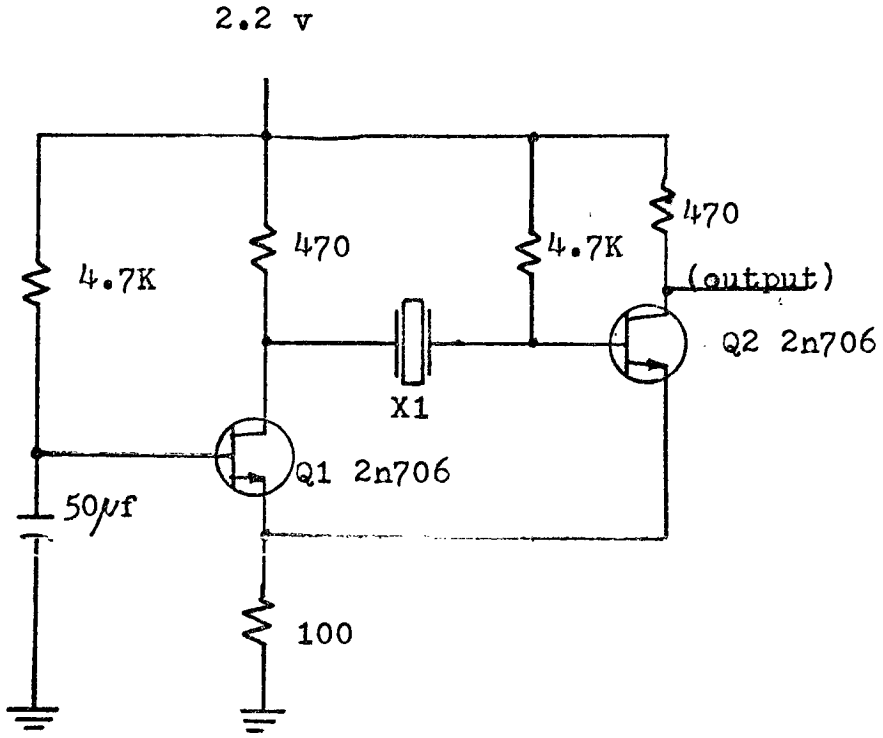
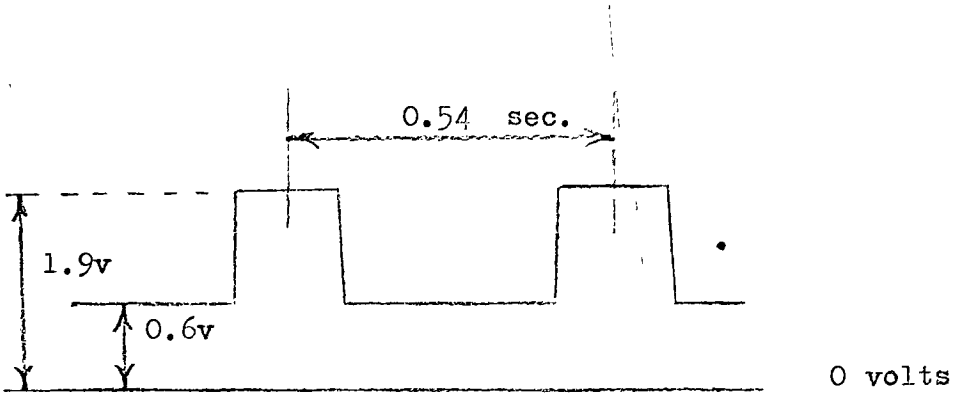


Figure 2 Oscillator



Frequency: 1851.00 KHZ

Risetime = Falltime: 40 nanosec.

Duty cycle: 50%

Figure 3 OSCILLATOR CHARACTERISTICS

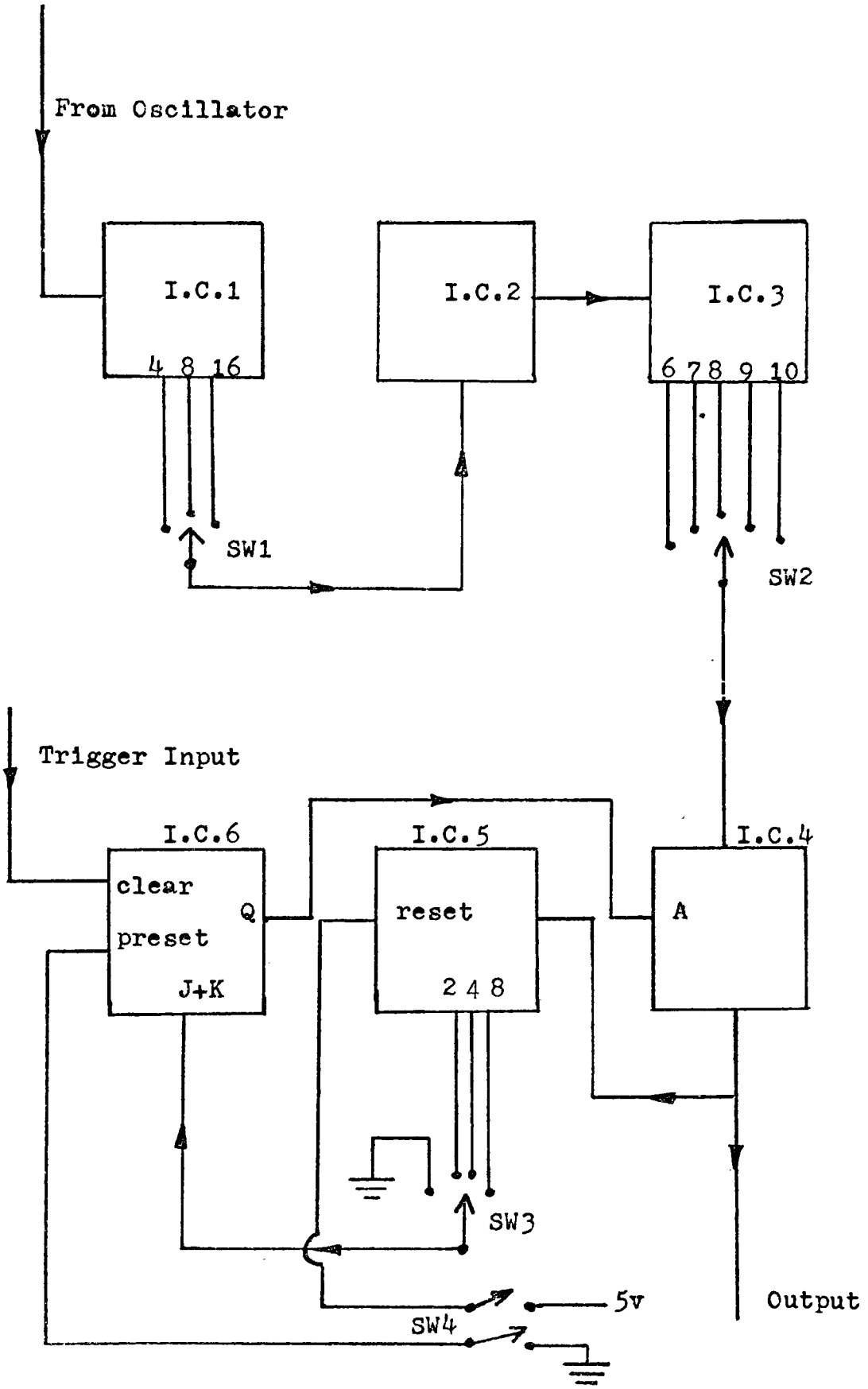
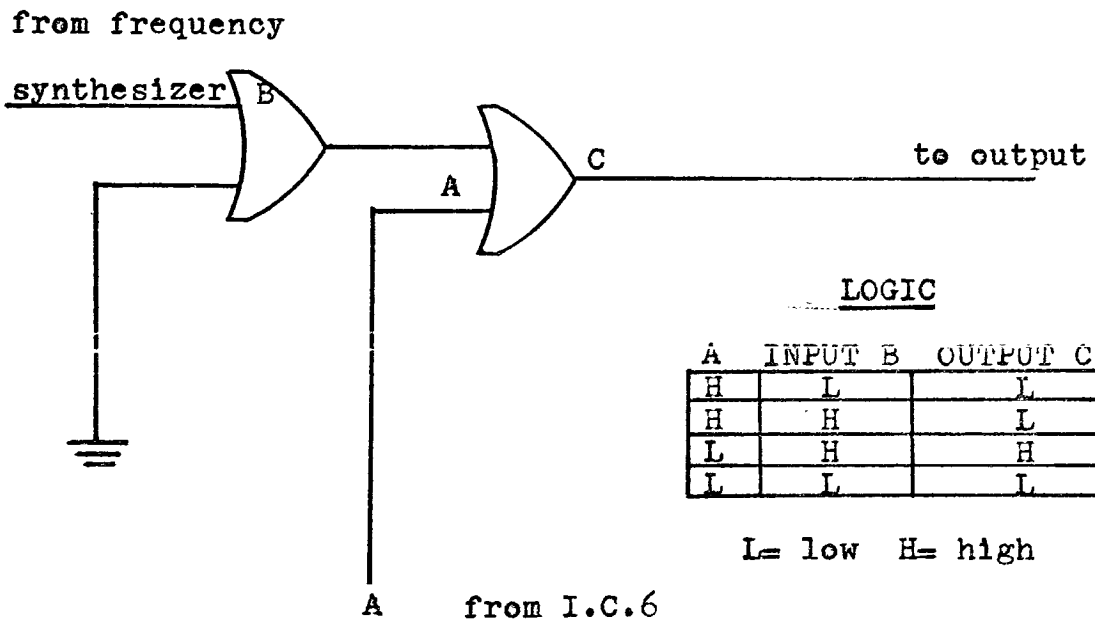


Figure 4 I.C. Board

TABLE 1

SWITCH POSITION SW1	SW2	FREQUENCY (KHZ)
A	1	723.0469
A	2	803.3854
A	3	903.8086
A	4	1032.9241
A	5	1205.0781
C	1	1446.0938
C	2	1606.7708
C	3	1807.6172
C	4	2065.8482
C	5	2410.1563
B	1	2892.1875
B	2	3213.5417
B	3	3615.2344
B	4	4131.6964
B	5	4820.3125



LOGIC

A INPUT B	OUTPUT C
H L	L
H H	L
L H	H
L L	L

L= low H= high

Figure 5 Nor Gate

the circuit is retriggered. Point A's logic is controlled directly by I.C.6, a edge triggered JK flip-flop which in turn is controlled by I.C.5, another 4 bit binary counter. Switch SW3 allows I.C.5 to count 2,4, 8 pulses or it may be grounded to allow free run operation. The trigger mechanism operates in the following manner; when the trigger button is depressed or a pulse is applied to the external trigger input, the clear input of I.C.6 goes low. This makes the Q output to go low and since this is attached to point A of I.C.4 pulses will be allowed to pass to the output. Each pulse that goes past the nor gate is counted by I.C.5 and when either 2, 4,8 pulses have been counted, depending on the position of switch SW3, I.C.5 presents a a high logic to the JK,preset inputs. I.C.6. This causes the Q output to go high again and since point A also goes high the flow of pulses is terminated until the circuit is retriggered. To prepare the circuit to be refired so that the counter is reset to zero the reset switch SW4 must be momentarily moved to the reset position and then back to count. While SW4 is in the reset position a low logic is applied to the reset input of I.C.5 causing the counter to return to zero and at the same time a high logic is applied to the preset input of I.C.6 to maintain its Q output high since it might be falsely triggered by the reset function of I.C.5. The circuit is now prepared to be fired again.

SUMMARY

At the last test the operating conditions were as follows;

Trigger: this circuit is fully operational, both the external trigger and trigger button are capable of firing the generator in the desired manner.
Counter: the counter was operating as desigined and along with the Nor gate was terminating the flow of pulses after the desired count.
Frequency Synthesizer: Due to the fact that a source of well shaped square waves was not avaiable it was not possible to exactly determine if the frequency division was being done as specified. However preliminary tests did show that divison was taking place at all settings.
Voltage Regulator: this circuit is capable of supplying the full 5 volts under all operating conditions of the I.C. circuit. In addition up to a 20% drop in line voltage was compensated for.
Oscillator: this is the only circuit that is not operational. At the last test no pulses were being generated.

LIST OF REFERENCES

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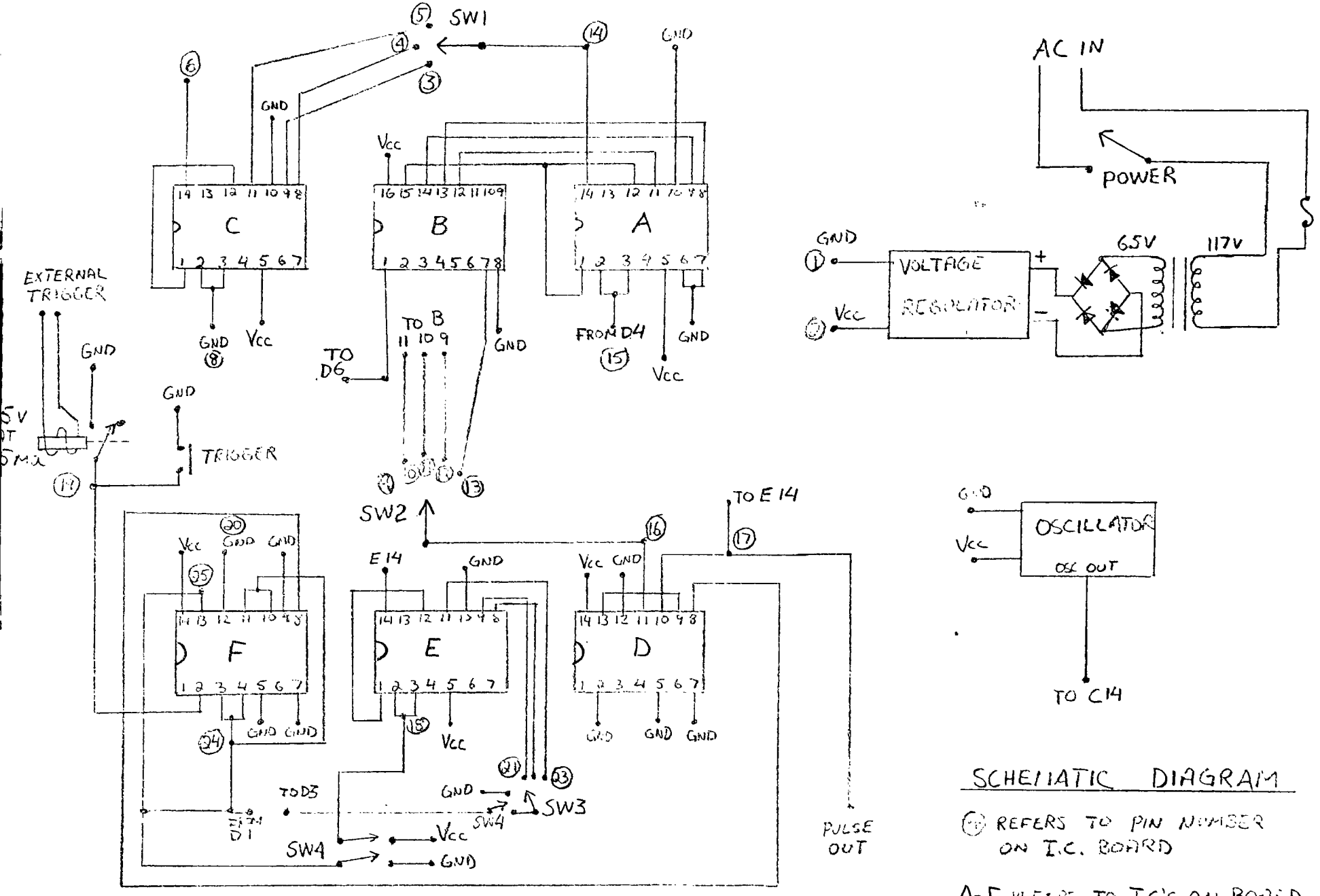
3. Markus John. Sourcebook of Electronic Circuits. New York: McGraw Hill, 1968
4. Gillie Angelo. Pulse and Logic Circuits. New York: McGraw Hill, 1968
5. Morris N.M. Logic Circuits. London: McGraw Hill,1969
6. Texas Instrument. TTL Intergrated Circuit Data. Catalog # CC201, 1968

APPENDIX



SCHEMATIC DIAGRAM

(14) REFERS TO PIN NUMBER ON I.C. BOARD

A-F REFERS TO IC'S ON BOARD

CIRCUIT TYPES SN5493, SN7493
4-BIT BINARY COUNTERS

MSI TTL HIGH-SPEED RIPPLE-THROUGH COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLE (See Notes 1, 2, and 3)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

NOTES: 1. Output A connected to input B
2. To reset all outputs to logical 0 both $R_{0(1)}$ and $R_{0(2)}$ inputs must be at logical 1.
3. Either (or both) reset inputs $R_{0(1)}$ and $R_{0(2)}$ must be at a logical 0 to count.

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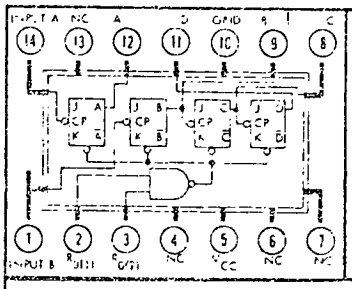
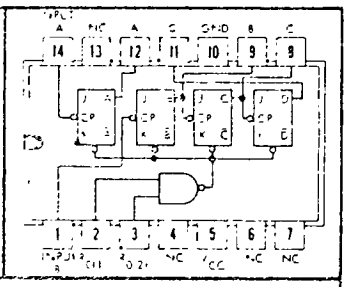
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC—No Internal Connection

description

These high-speed, monolithic 4-bit binary counters consist of four master-slave flip-flops which are internally interconnected to provide a divide-by-two counter and a divide-by-eight counter. A gated direct reset line is provided which inhibits the count inputs and simultaneously returns the four flip-flop outputs to a logical 0. As the output from flip-flop A is not internally connected to the succeeding flip-flops the counter may be operated in two independent modes:

1. When used as a 4-bit ripple-through counter, output A must be externally connected to input B. The input count pulses are applied to input A. Simultaneous divisions of 2, 4, 8, and 16 are performed at the A, B, C, and D outputs as shown in the truth table above.

2. When used as a 3-bit ripple-through counter, the input count pulses are applied to input B. Simultaneous frequency divisions of 2, 4, and 8 are available at the B, C, and D outputs. Independent use of flip-flop A is available if the reset function coincides with reset of the 3-bit ripple-through counter.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 32 mW per flip-flop (128 mW total).

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 4)		7 V
Input Voltage, V_{in} (See Notes 4 and 5)		5.5 V
Operating Case Temperature Range:	SN5493S	−55°C to 125°C
Operating Free-Air Temperature Range:	SN5493J, SN5493N	−55°C to 125°C
	SN7493 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 4. These voltage values are with respect to network ground terminal.
5. Input signals must be zero or positive with respect to network ground terminal

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 4): SN5493 Circuits	4.5	5	5.5	V
SN7493 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 6)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE: 6. Fan-out from output A to input B and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A or B inputs	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$ or $R_{0(2)}$ inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at A or B inputs	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out}=0	SN5493	−20		−57	mA
				SN7493	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5493		32	46	mA
				SN7493		32	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum frequency of input count pulses		C_L = 15 pF, R_L = 400 Ω	10	18		MHz
t_{pd1}	Propagation delay time to logical 1 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns
t_{pd0}	Propagation delay time to logical 0 level from input count pulse to output D	6	C_L = 15 pF, R_L = 400 Ω		75	135	ns

— SEE ORDERING INSTRUCTIONS PAGE 1-1 —

CIRCUIT TYPES SN5490, SN7490
DECADE COUNTERS

MSI TTL HIGH-SPEED DECADE COUNTERS

for applications in

- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLES

BCD COUNT SEQUENCE
(See Note 1)

COUNT	OUTPUT D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

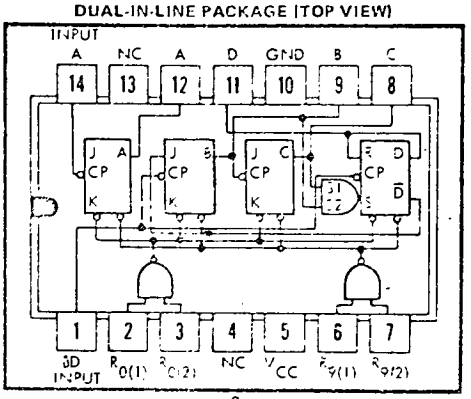
RESET/COUNT (See Note 2)

RESET INPUTS $R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	OUTPUT D C B A
1	1	0	X	0 0 0 0
1	1	X	0	0 0 0 0
X	X	1	1	1 0 0 1
X	0	X	0	COUNT
0	X	0	X	COUNT
0	X	X	0	COUNT
X	0	0	X	COUNT

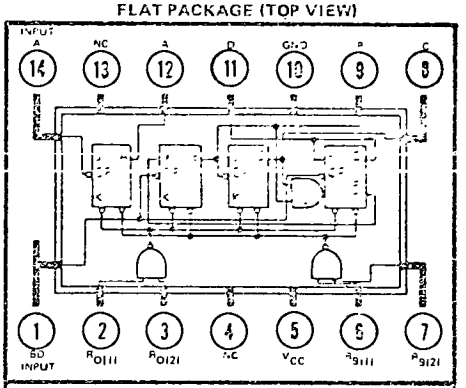
NC—No Internal Connection

NOTES: 1. Output A connected to input BD for BCD count.
2. X indicates that either a logical 1 or a logical 0 may be present.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



W
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

description and typical count configurations

These high-speed, monolithic decade counters consist of four dual-rank, master-slave flip-flops internally interconnected to provide a divide-by-two counter and a divide-by-five counter. Gated direct reset lines are provided to inhibit count inputs and return all outputs to logical zero or to a binary coded decimal (BCD) count of 9. As the output from flip-flop A is not internally connected to the succeeding stages, the count may be separated in three independent count modes:

1. When used as a binary coded decimal decade counter, the BD input must be externally connected to the A output. The A input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown above. In addition to a conventional zero reset, inputs are provided to reset a BCD count for nine's complement decimal applications.

2. If a symmetrical divide-by-ten count is desired for frequency synthesizers or other applications requiring division of a binary count by a power of ten, the D output must be externally connected to the A input. The input count is then applied at the BD input and a divide-by-ten square wave is obtained at output A.

3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The BD input is used to obtain binary divide-by-five operation at the B, C, and D outputs. In this mode, the two counters operate independently; however, all four flip-flops are reset simultaneously.

These circuits are completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is 160 mW.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 3) . . . . . 7 V
Input Voltage, V_{in} (See Notes 3 and 4) . . . . . 5.5 V
Operating Case Temperature Range: SN5490S . . . . . −55°C to 125°C
Operating Free-Air Temperature Range: SN5490J, SN5490N . . . . . −55°C to 125°C
SN7490 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5490 Circuits	4.5	5	5.5	V
SN7490 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output (See Note 5)			10	
Width of Input Count Pulse, $t_{p(in)}$	50			ns
Width of Reset Pulse, $t_{p(reset)}$	50			ns

NOTE 5. Fan-out from output A to input BD and to 10 additional Series 54/74 loads is permitted.

electrical characteristics (over operating temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input A	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at input BO	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at $R_{0(1)}$, $R_{0(2)}$, $R_{9(1)}$, or $R_{9(2)}$	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at input A	4	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at input BD	4	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX, V_{out} = 0 V	SN5490	−20		−57	mA
				SN7490	−18		−57	mA
I_{CC}	Supply current	3	V_{CC} = MAX, V_{in} = 4.5 V	SN5490		32	46	mA
				SN7490		32	53	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C
§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

TTL
MSI

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)

- BCD-to-Decimal
- Excess 3-to-Decimal
- Excess 3 Gray-to-Decimal

Also for applications as

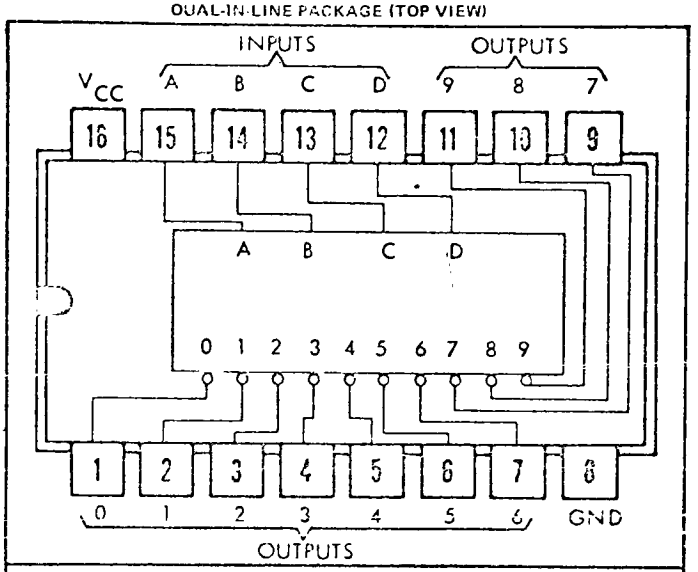
- 4-Line to 16-Line Decoders
- 3-Line to 8-Line Decoders
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess 3-to-decimal, and SN5444/SN7444 excess 3 gray-to-decimal decoders feature familiar transistor-transistor logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth tables

SN5442/SN7442 BCD INPUT				SN5443/SN7443 EXCESS 3 INPUT				SN5444/SN7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

CIRCUIT TYPES SN5442, SN5443, SN5444, SN7442, SN7443, SN7444
4-LINE-TO-10-LINE DECODERS (1-OF-10)

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5442, SN5443, SN5444 Circuits . . . . . −55°C to 125°C
SN7442, SN7443, SN7444 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions (over operating temperature range)

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5442, SN5443, SN5444 Circuits	4.5	5	5.5	V
SN7442, SN7443, SN7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output (N)			10	

electrical characteristics (over operating temperature range unless otherwise noted)

	PARAMETER	TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2	V_{CC} = MIN		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX,	SN5442, SN5443, SN5444	−20		−55	mA
				SN7442, SN7443, SN7444	−18		−55	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5442, SN5443, SN5444		28	41	mA
				SN7442, SN7443, SN7444		28	56	mA

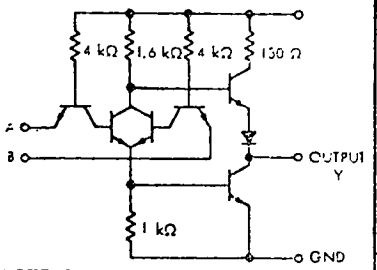
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

	PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		26	35	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

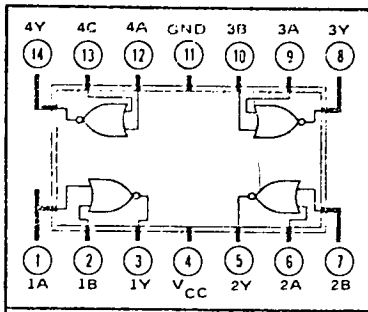
—SEE ORDERING INSTRUCTIONS PAGE 1-1—

schematic (each gate)

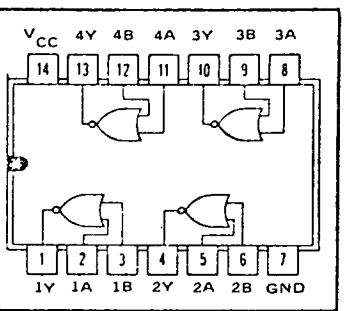


NOTE: Component values shown are nominal.

S FLAT PACKAGE
(TOP VIEW)



J OR N-DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{A + B}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5402 Circuits	4.5	5	5.5	V
	SN7402 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5402 Circuits	−55	25	125	°C
	SN7402 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at either input terminal to ensure logical 0 level at output	8	V_{CC} = MIN		2			V
$V_{in(0)}$	Logical 0 input voltage required at both input terminals to ensure logical 1 level at output	9	V_{CC} = MIN				0.8	V
$V_{out(1)}$	Logical 1 output voltage	9	V_{CC} = MIN, V_{in} = 0.8 V, I_{load} = −400 μA		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	10	V_{CC} = MIN, V_{in} = 2 V, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	11	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	12	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	13	V_{CC} = MAX	SN5402	−20		−55	mA
				SN7402	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	14	V_{CC} = MAX, V_{in} = 5 V			14	27	mA
$I_{CC(1)}$	Logical 1 level supply current	14	V_{CC} = MAX, V_{in} = 0			8	16	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF, R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF, R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

—SEE ORDERING INSTRUCTIONS PAGE 1-1—

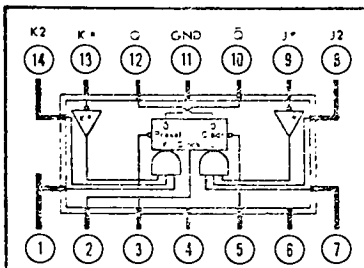
CIRCUIT TYPES SN5470, SN7470
EDGE-TRIGGERED J-K FLIP-FLOPS

logic

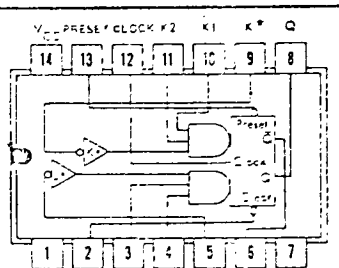
TRUTH TABLE		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. $J = J1 \cdot J2 \cdot \overline{J^*}$.
2. $K = K1 \cdot K2 \cdot K^*$.
3. t_n = Bit time before clock pulse.
4. t_{n+1} = Bit time after clock pulse.
5. If inputs J* or K* are not used they must be grounded.
6. NC - No Internal Connection

S FLAT PACKAGE
(TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: Low input to preset sets Q to logical 1
Low input to clear sets Q to logical 0
Preset or clear function can occur only when clock input is low.

description

These monolithic, edge-triggered J-K flip-flops feature gated inputs, direct clear and preset inputs, and complementary Q and $\overline{Q}$ outputs. Input information is transferred to the outputs on the positive edge of the clock pulse.

Direct-coupled clock triggering occurs at a specific voltage level of the clock pulse, and after the clock input threshold voltage has been passed, the gated inputs are locked out.

These flip-flops are ideally suited for medium- to high-speed applications and can result in a significant saving in system power dissipation and package count where input gating is required.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5470 Circuits	4.5	5	5.5	V
SN7470 Circuits	4.75	5	5.25	V
Operating Free-Air Temperature Range, T_A: SN5470 Circuits	−55	25	125	°C
SN7470 Circuits	0	25	70	°C
Normalized Fan-Out From Each Output, N			10	
Clock Pulse Transition Time to Logical 1 Level, $t_{1(clock)}$ (See Figure 68)			150	ns
Width of Clock Pulse, $t_{p(clock)}$ (See Figure 68)	20			ns
Width of Preset Pulse, $t_{p(preset)}$ (See Figure 67)	25			ns
Width of Clear Pulse, $t_{p(clear)}$ (See Figure 67)	25			ns

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	36 and 37	V_{CC} = MIN			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	36 and 37	V_{CC} = MIN					0.8	V
$V_{out(1)}$	Logical 1 output voltage	36	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	37	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J1, J2, J*, J1, K2, K*, or clock	38	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset or clear	38	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J1, J2, J*, K1, K2, K*, or clock	39	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset or clear	39	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	40	V_{CC} = MAX,	V_{in} = 0	SN5470	−20		−57	mA
					SN7470	−18		−57	
I_{CC}	Supply current	39	V_{CC} = MAX,	V_{in} = 5 V			13	26	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{clock}	Maximum clock frequency	68	C_L = 15 pF,	R_L = 400 Ω	20	35		MHz
t_{setup}	Minimum input setup time	68	C_L = 15 pF,	R_L = 400 Ω		10	20	ns
t_{hold}	Minimum input hold time	68	C_L = 15 pF,	R_L = 400 Ω		0	5	ns
t_{pd1}	Propagation delay time to logical 1 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level from clear or preset to output	67	C_L = 15 pF,	R_L = 400 Ω			50	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	68	C_L = 15 pF,	R_L = 400 Ω	10	27	50	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	68	C_L = 15 pF,	R_L = 400 Ω	10	18	50	ns